RAHUL MACHA

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PROFESSIONAL SUMMARY

Design Verification Engineer skilled in Verilog, SystemVerilog, UVM, functional verification, SVA, functional coverage, QuestaSim, and Synopsys Verdi. Experienced in developing self-checking testbenches and verifying RTL/protocol behavior through simulation, waveform analysis, and debugging in a Linux environment. Project experience includes AMBA APB and 10G Ethernet MAC TX verification.

EDUCATION

Bharat Institute of Higher Education and Research **Sep 2022 - May 2026**

B.Tech, Electronics and Communication Engineering **CGPA: 8.32**

TECHNICAL SKILLS

HDL:	Verilog, SystemVerilog
Verification:	Testbench Development, Constrained Random Verification, Functional Coverage, SystemVerilog Assertions (SVA), Scoreboards, Monitors, Drivers
UVM:	UVM Architecture, Sequencer, Sequences, Factory, Configuration Database, TLM, Driver, Monitor, Agent, Scoreboard
Simulation & Debug:	QuestaSim, Synopsys Verdi, Waveform Analysis, RTL Debugging
Protocols:	AMBA APB, Ethernet / MAC
Operating System:	Linux
Version Control:	Git, GitHub
Programming:	C, Python

PROJECTS

10G Ethernet MAC (10GEMAC) – TX Loopback Mechanism Verification | SystemVerilog, UVM, QuestaSim, Verdi, Linux

- Built a UVM environment for a 10G Ethernet MAC (64-bit XGMII) with TX/RX agents, scoreboard, coverage and SVA; verified 1,000+ packets via TX-to-RX loopback.
- Wrote the verification plan from the spec alone, treating the DUT as a black box (requirements, architecture, coverage and test plans).
- Created 15+ directed and constrained-random tests (64B–1518B, runt/jumbo, 96-bit IFG, CRC/FCS) and 20+ SVA checks, reaching 96%+ functional coverage.
- Debugged with QuestaSim/Verdi waveforms; found a duplicated preamble in stimulus and an XGMII control-bit width mismatch.

APB Protocol Slave Verification | Verilog, SystemVerilog, UVM, QuestaSim, Synopsys Verdi, Linux

- Developed a UVM-based self-checking testbench for APB slave verification, integrating sequences, sequencer, driver, monitors, and scoreboard.
- Generated directed and configurable read/write transactions using random, incrementing, decrementing, constant, and predefined address/data patterns.
- Implemented SystemVerilog Assertions (SVA) to verify APB protocol sequencing, signal stability, reset behavior, and transfer-phase requirements.
- Developed functional coverage models to track address, write-data, read/write control signals, and key protocol scenarios.
- Analyzed simulation waveforms, debugged protocol violations, and evaluated verification results using QuestaSim and Synopsys Verdi.

CERTIFICATIONS

Design Verification Training - VLSI FIRST (Feb 2026 - Aug 2026)

(Verilog | SystemVerilog | SVA | Functional Coverage | UVM | QuestaSim)

Completed hands-on training in digital design and functional verification, covering Verilog HDL, RTL design concepts, and testbench development using QuestaSim, with applied practice through protocol- and MAC-level